

Reg No.: \_\_\_\_\_

Name: \_\_\_\_\_

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  
**SIXTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), MAY 2019**

**Course Code: EC304**

**Course Name: VLSI**

Max. Marks: 100

Duration: 3 Hours

**PART A**

*Answer any two full questions, each carries 15 marks*

Marks

- |   |  |      |
|---|--|------|
| 1 | a) How electronic grade silicon is prepared from raw SiO <sub>2</sub> ?  | (5)  |
|   | b) Illustrate the dry and wet oxidation technique used in IC fabrication with schematic diagram.   | (10) |
| 2 | a) With the help of mathematical equations, explain the distribution of impurities in a semiconductor in ion implantation process.   | (10) |
|   | b) Phosphorous is implanted in a p-type silicon sample with a uniform doping concentration of $5 \times 10^{16}$ atoms per cm <sup>3</sup> . If the beam current density is 2.5μA per cm <sup>2</sup> and the implantation time is 8 minutes, calculate the implantation dose and peak impurity concentration. Assume $\Delta R_p = 0.3 \mu\text{m}$ | (5)  |
| 3 | a) Explain N-well CMOS IC fabrication sequence with the help of neat diagrams.   | (10) |
|   | b) Explain one method of fabrication of capacitor structure in integrated circuits.  | (5)  |

**PART B**

*Answer any two full questions, each carries 15 marks*

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|---|---|------|
| 4 | a) Explain the various types of power dissipation in CMOS inverter? Derive the expression for total power consumption of a CMOS inverter. | (10) |
|   | b) Why PMOS transistor can pass only strong ones and NMOS can pass strong zeros.  | (5)  |
| 5 | a) Draw the circuit diagram and layout of a two input CMOS NAND gate.   | (10) |
|   | b) Implement the function $u = A'B + AB'$ and $v = AB + A'B'$ using complementary pass transistor logic.                                  | (5)  |
| 6 | a) Explain the structure and working of a transmission gate.<br>Implement 4×1 multiplexer using transmission gates.                       | (10) |
|   | b) Implement the function $f = [AB + C (DE + F)]'$ using static CMOS logic.   | (5)  |

**PART C**

*Answer any two full questions, each carries 20 marks*

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|---|--|------|
| 7 | a) Explain the read and write operation of a six transistor CMOS SRAM cell.                        | (10) |
|   | b) What is FPGA? Explain its constructional details with diagram. What are the advantages of FPGA? | (10) |
| 8 | a) Design a 4-bit × 4-bit NOR-based ROM array and explain its working.                             | (10) |
|   | b) Explain the read and write operation of a three-transistor DRAM cell.                           | (10) |
| 9 | a) Explain the working a 16-bit carry-by pass adder and write down the expression                  | (10) |

for worst-case delay.

- b) Explain 4×4 bit-array multiplier with block diagram.

(10)

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